REMARKS

I. Status of the Application

In the Office Action mailed September 18, 2006, the Examiner objected to page 26 of the specification due to an error in the description of a figure. The Examiner maintained all rejections of claims 1-4, 6, 8-9, 25-28 and 30 under 35 USC § 102(b) as being anticipated by US Patent 6,161,210 to Chen *et al.* ("Chen"), and rejected claims 13-22 and 24 as being anticipated by the reference "Algorithm-based low-power and high-performance multimedia signal processing" by Liu ("Liu"). The Examiner also rejected claims 5, 7, 10, 12, 23 and 29 under 35 USC § 103 based on either the Chen or Liu references in combination with one or more of US Patent 6,070,263 to Tsui ("Tsui"), the reference "A Transformation for Computational Latency Reduction in Turbo-MAP decoding" to Raghupathy, and the reference "High-performance VLSI architecture for the Viterbi Algorithm" to Boo ("Boo").

Applicants herein have amended the specification and claims, and respectfully request reconsideration in view of the following remarks.

II. Examiner Interview

Applicants would like to thank the Examiner for the interview conducted on November 2, 2006. Participating in the interview with the Examiner were Dr. Naresh Shanbhag (Applicant) and Mr. Robert Irvine (Applicants' representative). The Chen prior art reference was discussed, and Applicants argued that the concept of "time-reverse" path identification used in claims 2, 15, 19 and 26 was not disclosed. Applicants also described how the Parallel architecture claimed in claims 9, 14, 16 and 17 was not present in the cited references. Agreement with respect to the claims was not reached.

III. Response to the Office Action

A. The Specification

Applicants have amended paragraph 58 in accordance with the Examiner's suggestion. Applicants submit that no new matter has been added, as the amendment is clearly supported by the specification and Figures.

B. Response to the Rejections

Presently pending are claims 1, 3-14, 16-18, 20-25, and 27-30, of which claims 1, 9, 13, 16, 17, and 25 are independent claims,

Applicants have amended claims 1, 13, and 25 to incorporate the element of time-reverse candidate path identification. The prior art of record does not describe time-reverse path identification. The specification includes embodiments having a compare-select-add circuit, shown in Figure 8, and described in the application in paragraphs 24 and 58, and in great detail in paragraphs 59-60. In these embodiments, time reverse candidate path selection is performed by comparing paths starting at the *ends* of *the possible paths in the group*. The grouping of paths makes the time-reverse comparison of the paths possible because the paths in the group can be paired in a way that they differ only at the ends of the paths. For at least this reason, Applicants submit that claims 1, 13, and 25 are allowable. Applicants further submit that those claims depending from independent claims 1, 13, and 25 are also allowable.

Applicants submit that the remaining independent claims (9, 16, and 17) all include a parallel architecture that is not shown in any of the cited references. The architecture described in the specification depicts numerous blocks that operate in parallel to identify the best paths, and whose outputs are strung together such that the decision outputs of one are fed into another to select the output of that block. See Figure 6, and the discussion at

paragraphs 53 and 54. This type of independent processing by the CPI blocks, followed by interconnected or cascaded candidate path selection via the mux devices is not present in the prior art of record.

The aspect of interconnected parallel blocks is present in at least independent claims 9 (operating on at least two sets of data, and using the output of one to select the output of the other), 16 (a "plurality of candidate path identification blocks" and a plurality of "selection devices", and wherein "the data outputs of each of said plurality of selection devices is used to select the data outputs of another of said plurality of selection devices"), and 17 (where the output decision information of a selecting means is generated in response to output decision information from a selecting means of another decoding means).

Thus, Applicants respectfully traverse the rejections because the Examiner has not established that the references teach each and every element of any of these claims as would be required to support an anticipation rejection under M.P.E.P. § 2131.

IV. Conclusion

The Applicants submit that the application is in good and proper form for allowance and respectfully request the Examiner to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney, at 312-913-3305.

Respectfully submitted,

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Date: November 20, 2006 By: /Robert J. Irvine III/

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